applying a first ac signal to the first input terminal of a single-stage analog multiplier having a first input terminal, a second input terminal and an output terminal;

setting the output terminal of said single-stage analog multiplier to ac zero; and

outputting a [quadrature] second ac signal at quadrature with said first ac signal from a second [multiplicand] input terminal of said analog multiplier.

Claim 17. (new) The quadrature frequency generator as described in claim 2, wherein said ac short-circuit is provided with a capacitor.

REMARKS

Claims 1 and 15 have been canceled. Claims 2-4 and 16 have been amended. Claims 12-14 have been withdrawn. Claim 17 has been added. Claims 5-11 remain unchanged.

The Examiner objected the informalities on page 3, line 20, citing that "PMOS current mirror M3 and M4" should be changed to --PMOS current mirror M4 and M5--. In addition, it has been found that "M2 and M4" were also mistyped, and should be corrected as --M3 and M5--. The word "V_{Bias}" should be deleted, because it is not labeled in Fig.4. The specification has been changed according to the Examiner's suggestion and our findings. No new matter has been introduced.

The Examiner objected to claim 1 for the informalities of the misspelled word "multiplicant". This word has been deleted.

The Examiner rejected claim 1-11 under 35 U.S.C. 112 as being indefinite , citing that "the second multiplicand is misdescriptive". Claim 1 has been canceled. Claim 2 has been rewritten to be the independent claim. The indefinite description has been corrected by deleting the word "multiplicand" and describing the multiplier to comprise: a first input terminal, a second input terminal, and an output terminal. The first ac input signal (i.e. the in- phase signal) is applied to the first input terminal , the output terminal is ac shorted, and the quadrature ac signal is outputted from the second input terminal. With this amended description, it is believed that claim 2 and its dependent claims 3-11 are no longer indefinite.

The Examiner rejected claims 1-11 under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,659,263, issued to Dow et al. Dow described in Column 4, lines 8-10, a prior art Gilbert multiplier circuit shown in his Fig. 2 that "the output signal VPHASE has a magnitude of zero when input signal VIN and VQUAD are in quadrature". However, "zero magnitude" does not necessarily mean a short-circuit. Dow did not show that by setting the output to be zero with an ac short-circuit and applying an in-phase signal to one of the input terminals, a quadrature signal can be outputted from

the other input terminal. To derive an output signal from an input terminal is not expected by a person skilled in the art, and Dow did not disclose this feature. Nor did Dow disclose any short-circuit and means to short circuit (i.e. capacitor) the output in any of his figures. As a matter of fact, no capacitor is shown in any of Dow's figures. Therefore Dow did not teach the key points of the present invention: the ac short-circuited output terminal and deriving a quadrature output signal from an input terminal. These features are highlighted in the rewritten claim 2 with these limitations. An additional claim 17 has been added to stress the use of capacitor to ac short- circuit the output terminal of the multiplier. Other Dow's figures show multi-stage block diagrams, which are totally different from the single-stage multiplier of the present invention and further teach away from the present invention. By limiting the multiplier to be single-stage, claims 2 and 16 are all the more not anticipated by Dow. With these added limitations and claim, it is believed that claims 2 with its dependent claims 3-11, 17 and the corresponding method claim 16 are no longer anticipated by Dow.

In view of the above, it is submitted that claims 2-11, 16, as amended, and claim 17, as added, are in condition for allowance. Reexamination of the objections and rejections is requested. Allowance of claims 2-11, 16 and 17 at an early date is solicited.

Respectfully submitted,

Hung Chang Lin

Hung Chang LIN, Patent Agent Registration No.28789
8 Schindler Court, Silver Spring, MD 20903
Telephone: 301-434-3571

Certificate of Mailing

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

Hung Chang LIN	(Depositor's name)
Hung Chang Lin	(Signature)
4/21/04	(Date)